Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV (New) EXAMINATION – WINTER 2019

Subject Code: 2140707 Date: 13/12/2019

Subject Name: Computer Organization

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Explain following terms: 1) Micro-Operation 2) Micro-instruction 3) Pseudo instruction.	**03**
	(b)	Draw a diagram of 4-bit binary incrementer and explain it briefly.	**04**
	(c)	List and explain any seven addressing mode.	**07**
Q.2	**(a)**	Write a truth table of three state buffer and explain high impedance state in it with logic symbol diagram.	**03**
	(b)	What is Flynn's taxonomy? Explain it in brief.	**04**
	(c)	Explain shift micro-operations with necessary diagrams.	**07**
		OR	
	(c)	Draw and explain a flowchart of interrupt cycle.	**07**
Q.3	**(a)**	Write micro-instruction format and give one example.	**03**
	(b)	Briefly explain any four characteristics of RISC.	**04**
	(c)	What is role of first pass assembler? Explain assembler's second pass with flowchart.	**07**
		OR	
Q.3	**(a)**	What is overlapped register window in RISC?	**03**
	(b)	Draw and explain flow chart of address sequencing.	**04**
	(c)	Explain Design of Control Unit with block diagram.	**07**
Q.4	**(a)**	Explain the following instructions: CIL, SNA, INP.	**03**
	(b)	Explain memory interleaving.	**04**
	(c)	Name various CPU organizations and explain any one in detail.	**07**
		OR	
Q.4	**(a)**	What are the various ways to handle branch difficulties? Explain any one in detail.	**03**
	(b)	Explain crossbar switch interconnection structures.	**04**
	(c)	Explain array multiplier with logic diagram.	**07**
Q.5	**(a)**	Describe following: 1) Locality of reference 2) Cache memory 3) Hit ratio.	**03**
	(b)	Write a short note on DMA.	**04**
	(c)	Explain Booth Multiplication Algorithm with example.	**07**
		OR	
Q.5	**(a)**	Differentiate isolated I/O and Memory mapped I/O.	**03**
	(b)	List and describe dynamic arbitration algorithms.	**04**
	(c)	What is cache memory mapping? Explain direct cache memory mapping in detail.	**07**

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